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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,343	02/06/2004	Paul R. Sharps	1613370-0046 CON	6467

7590 08/05/2005

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EXAMINER	
DIAMOND, ALAN D	

ART UNIT	PAPER NUMBER
1753	

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,343	SHARPS ET AL.	
	Examiner	Art Unit	
	Alan Diamond	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *37-73 and 86-111* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37-73 and 86-111* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

LR

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 20, 2005 has been entered.

Comments

2. The Examiner acknowledges that the continuity data for Serial No. 10/280,593 has been updated.

3. The objection to the disclosure for informalities has been overcome by Applicant's amendment thereof.

4. The Examiner acknowledges that claims 74-85 have been canceled.

5. The Examiner notes that claim 93 has been amended in accordance with the language suggested by the Examiner at the bottom of page 3 of the Final Rejection mailed January 4, 2005.

6. The 35 USC 112, first paragraph, rejection of claims 88 and 101-111 has been overcome by Applicant's of parent claim 86 so as to change "first portion" to "second portion" at line 5.

7. The 35 USC 112, second paragraph, rejection of the claims has been overcome by applicant's amendment of the claims, other than the rejections set forth below.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 37-46, 50-64, and 90-92 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In claim 37, at line 5, the term "identical sequences of layers", i.e., plural identical sequences without any recitation as to what the layers are made from, is not supported by the specification, as originally filed. The same applies to dependent claims 38-46. It is suggested that said term be changed to "an identical sequence of semiconductor layers".

In claim 37, at lines 5-6, the "substantially the same thickness" limitation is not supported by the specification, as originally filed. The same applies to dependent claims 38-46.

In claim 47, the requirement that the top layer of the top cell has a first polarity and the bottom layer of the bypass diode has said first polarity is not supported by the specification, as originally filed.

In claim 45, at line 2, the "as least in part" (presumably "at least in part") range for the InGaP is not supported by the specification, as originally filed.

In claim 46, at line 2, the "at least in part" range for the GaAs is not supported by the specification, as originally filed.

In claim 50, at line 9, the term "identical sequence of layers", i.e., a sequence without any indication as to what the layers are made from, is not supported by the specification, as originally filed. The same applies to dependent claims 51-64. It is suggested that said term be changed to "an identical sequence of semiconductor layers".

In claim 50, at lines 9-10, the "substantially the same thickness" limitation is not supported by the specification, as originally filed. The same applies to dependent claims 51-64.

In claim 90, the requirement that the top layer of the top cell has a first polarity and the bottom layer of the bypass diode has said first polarity is not supported by the specification, as originally filed. The same applies to dependent claims 91 and 92.

In claim 90, at line 9, the range of "at least one layer" for the bypass diode is not supported by the specification, as originally filed. The same applies to dependent claims 91 and 92.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 37-46, 50-64, and 94 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 37, at lines 5-6, it is not clear what is to be encompassed by the term "substantially the same thickness". The same applies to dependent claims 38-46.

In claim 45, at line 2, it is not clear what is meant by "as least in part".

Claim 50 is indefinite because it is not clear which of the plural subcells at line 4 is being referred to by the term "the subcell" at line 9 of claim 50. The same applies to dependent claims 51-64.

In claim 50, at lines 9-10, it is not clear what is to be encompassed by the term "substantially the same thickness". The same applies to dependent claims 51-64.

Claim 94 is indefinite because "said lateral conduction layer in the second region" at lines 1-2 lacks positive antecedent support in claim 93.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 47-49, 90-93, 95-98, 107, and 110 are rejected under 35 U.S.C. 102(e) as being anticipated by Boutros et al, U.S. Patent 6,635,507.

As seen in Figure 8, and with respect to independent claims 93 and 107, Boutros et al teaches a multijunction solar cell comprising a Ge substrate (802); a first region

including the N and P GaAs layers (804) which form a first junction of the multijunction solar cell and the N and P GaInP layers (806) which form a second junction of the multijunction solar cell, wherein this first region includes the portion of said N and P GaAs layers (804) and the portion of the N and P GaInP layers (806) not directly below, but to the right of the GaAs cap layer. In a second region, the portions of corresponding N and P GaAs layers (804) and N and P GaInP layers (806) directly below the GaAs Cap support the bypass diode (810) to protect the cell against reverse biasing (see also col. 1, lines 16-22; and col. 7, lines 47-65). With respect to claims 47 and 90, these claims require that the top layer of the top cell has a first polarity and that the bottom layer of the bypass diode has the first polarity. In Figure 8, it is the Examiner's position that the GaAs N^{++} layer can be considered to by the lower layer of the bypass diode, and thus, has the same polarity as the upper N-type GaInP layer of the upper solar cell. Indeed, as seen in Boutros et al's Figures 2A, 3A, and 4A, the bottom layer of the bypass diode (210, 310, 410) is N^{++} and is the same polarity, i.e., N-type, as the top layer (208, 308, 408) of the solar cell. With respect to claims 97 and 107, when the GaAs P^{++} layer is considered the lateral conduction layer (as per instant claims 96 and 110), then the bypass diode above it reads on the instant etch stop layer. Alternatively, with respect to claim 97 and 107 when the GaAs Cap N^{++} layer is considered the lateral conduction layer, then the GaAs P^{++} layer reads on the instant etch stop layer.

With respect to claim 98, and as clearly seen in said Figure 8, the Ge substrate (802) forms an electrical connection path between the multijunction solar cell and the bypass diode.

In an alternative with respect to claim 107, the N and P GaAs layers (804) and N and P GaInP layers (806) encompass the instant first region, and the bypass diode (810) encompasses the instant second sequence of layers.

Since Boutros et al teaches the limitations of the instant claims, the reference is deemed to be anticipatory.

14. Claims 37-41, 43, 44, 47, 48, 65, 66, 68, 69, 86, 87, 89-91, 93, 95, 97-101, 103, 104, and 106-108 are rejected under 35 U.S.C. 102(b) as being anticipated by JP 9-64397, herein referred to as JP '397.

JP '397's solar module in Figure 2 comprises a conductive substrate (203); a multijunction solar cell (201) having first (204A, 205A, 206A) and second (204B, 205B, 206B) subcells formed on a first portion of the substrate; bypass diode (202) formed on a second portion of the substrate (203) having p-type, i-type and n-type layers (205A, 204B, 207D); and metal contact layers (208, 208D) (see also paragraphs 0031 to 0045). As seen in Figure 2, the bypass diode (202) is clearly integral with and laterally spaced apart from both the first and second subcells. With respect to the limitation in claim 37 that the bypass device and the subcell have identical sequences of layers with substantially the same thickness and form an integral semiconductor body, it is seen that JP '397's multijunction solar cell solar cell in Figure 1 has transparent electrode (107) followed by collection electrode (108). This is the same sequence as in the bypass diode, which has transparent electrode (107D) followed by collection electrode (108D). JP '397's multijunction solar cell and bypass diode form an integral semiconductor body on the substrate (103). With respect to independent claims 47 and

90, the top layer (104A) of the top cell in Figure 1 can be p-type, and the bottom layer (104D) of the bypass diode can also be p-type (see paragraphs 0033, 0034, and Example 2 where a pinpin structure is used for the multijunction solar cell, i.e., layer 104A is p-type, and the bypass diode is ip structure, i.e., layer 104D is p-type). With respect to claim 93, JP '297's conductive substrate (103) in Figure 1 reads on the instant planar lateral conduction layer. With respect to claim 100, JP '397's Figures 1 and 2 anticipate this claim because a "corresponding" sequence encompasses the situation in these figures. In particular, each layer in the bypass diode has a "corresponding" layer in the multijunction solar cell in said figures. With respect to claim 107, as seen in JP '397's Figure 3, there is a substrate (303) that has a sequence of semiconductor layers, the lower portion of the sequence, i.e., layers (304A) to (306B) that forms the multijunction solar cell, and the upper portion of the sequence, i.e., layers (350D, 304D) that forms the bypass diode. In said Figure 2, conductive layer 308 reads on the instant highly conductive layer.

With respect to claim 39, Figure 3 of JP '397 shows another embodiment of the solar module. In this embodiment, the bypass diode (302) is grown over the layers of the subcells. The bypass diode (302) is integral with at least the subcell (304A,305A,306A) since said subcell (304A,305A,306A) and bypass diode (302) are both integral with the substrate (302) (see Figure 3).

With respect to claims 41 and 43, the contact (108D,208D,308D) is metal (see paragraph 0040), and it is the Examiner's position forms a metal/semiconductor Schottky junction as here claimed.

With respect to claim 44, the substrate can be considered to be lower-most semiconductor layer (204A,304A), which can contain Ge (see paragraph 0037).

With respect to claims 48 and 91, as clearly seen in Figure 2, the sequence of layers of the subcells and the sequence of layers of the bypass diode would clearly be grown in the same process step.

With respect to claims 65, 86, 99, and 108, the metal lead wire (209,309) together with the metal contact (208D,308D) read on the instant metal contact.

With respect to claims 66, 93, 100, and 107, the substrate (303) is also a lateral conduction layer. With respect to claim 95 and in the alternative, the lateral conduction layer can be considered to be semiconductor layer (304A), which is doped either n-type or p-type (see paragraph 0025).

With respect to claim 68 and 97, any of the layers (304A to 307) above the substrate (303), or any of the layers (305A to 307) above layer (304A) reads on the instant stop etch layer.

With respect to claim 89, as clearly seen in Figure 3, the sequence of layers of the subcells and the sequence of layers of the bypass diode would clearly be grown in a different, subsequent process step.

Since JP '397 teaches the limitations of the instant claims, the reference is deemed to be anticipatory.

15. Claims 47-57, 59, 61, 65-68, 70, and 86-111 are rejected under 35 U.S.C. 102(b) as being anticipated by Ho et al, WO 99/62125. In particular, see Figures 12 and 14B, and page 8, lines 16-23, which teach the claimed invention.

Ho et al's multijunction solar cell has a first portion at the left having a first GaAs subcell (1412-1416) and a second GaInP subcell (1422-1426); and a second portion laterally spaced apart from the first portion by a trough and including bypass diode (1410) that is integral with said first subcell (see Figure 14B; and page 8, lines 18-23). The diode (1410) includes a metal/semiconductor contact comprising front metal contact (1440), which, it is the Examiner's position, forms a Schottky junction with the tunnel diode layer N^{++}. The solar cell has a Ge substrate (1402-1404) (see Figure 14B). The combination of Ho et al's metal contact (1436) and front metal contact (1440) reads on the instant metal layer. The tunnel diode layers (1418) and (1420) in both said first and second portions in said Figure 14B read on the instant lateral conduction layer. With respect to claims 47 and 90, as seen in Ho et al's 14B, the top layer of the top cell is n-type GaAs layer (1412) which is of the same polarity as the bottom n^{++} tunnel diode layer (1420) of the bypass diode (1410). With respect to claim 50, the bypass diode and the GaAs subcell have the same sequence of layer an substantially the same thickness, as seen in said Figure 14B. With respect to claim 86, said Figure 14B clearly has first and second portions, the first portion having the solar cells, and the second portion having the overlying bypass diode (1410). With respect to claim 93, the front metal contact (1440) in said Figure 14B reads on the instant planar lateral conduction layer. With respect to claim 100, as seen in said Figure 14B, front metal (1436) is a lateral conduction layer that is physically separated from front metal (1440), which is another lateral conduction layer. With respect to claim 107, see Ho et al's Figure 12, where there is a cascade solar cell at a lower portion, a bypass diode (1214, 1216) at

an upper portion, GaAs connecting layer (1210) which reads on the instant highly conductive lateral conduction layer, and layer (1222) which corresponds to the metal layer in instant claim 108 (see also page 7, line 16). The solar cell can be multijunction (see page 5, lines 15-20). Since Ho et al teaches the limitations of the instant claims, the reference is deemed to be anticipatory.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 47-68, 70, and 86-111 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boutros et al, U.S. Patent 6,635,507.

As seen in Figure 8, and with respect to independent claims 47, 65, 86, 90, 93 and 107, Boutros et al teaches a multijunction solar cell comprising a Ge substrate (802); a first region including the N and P GaAs layers (804) which form a first junction of the multijunction solar cell and the N and P GaInP layers (806) which form a second junction of the multijunction solar cell, wherein this first region includes the portion of said N and P GaAs layers (804) and the portion of the N and P GaInP layers (806) not directly below, but to the right of the GaAs cap layer. In a second region, the portions of corresponding N and P GaAs layers (804) and N and P GaInP layers (806) directly below the GaAs Cap support the bypass diode (810) to protect the cell against reverse biasing (see also col. 1, lines 16-22; and col. 7, lines 47-65). Said first and second

regions in said Figure 8 clearly are laterally spaced apart, as in claims 47 and 90. With respect to claims 66, 68, 70, 97, 107, when the GaAs P^{++} layer is considered the lateral conduction layer, then the bypass diode above it reads on the instant etch stop layer. Alternatively, with respect to claims 97 and 107 when the GaAs Cap N^{++} layer is considered the lateral conduction layer, then the GaAs P^{++} layer reads on the instant etch stop layer. As seen in Figure 8, there is a connecting electrical contact (816) deposited on a portion of the substrate (802) and over a portion of the bypass diode (i.e., over a portion of the second region). Clearly, this electrical contact is for shorting the multijunction solar cell (in both regions) and to electrically connect to said bypass diode in the second region.

With respect to claims 47 and 90, these claims require that the top layer of the top cell has a first polarity and that the bottom layer of the bypass diode has the first polarity. In Figure 8, it is the Examiner's position that the GaAs N^{++} layer can be considered to by the lower layer of the bypass diode, and thus, has the same polarity as the upper N-type GaInP layer of the upper solar cell. Indeed, as seen in Boutros et al's Figures 2A, 3A, and 4A, the bottom layer of the bypass diode (210, 310, 410) is N^{++} and is the same polarity, i.e., N-type, as the top layer (208, 308, 408) of the solar cell.

With respect to claims 48 and 91, when Boutros et al's sequential deposition steps (col. 8, lines 4-46) are considered a growth step, then the layers of the multijunction solar cell and bypass diode are grow sequentially in the same process step, i.e., the process step is the sequential growth of the layers. After the growth step, there is etching (see col. 8, lines 37-46).

With respect to claim 89, and in an alternative with respect to the immediately preceding, the first and second solar cells (804,806) can be considered to be grown in a first process, and then the bypass diode (810) can be considered to be grown in a second process after the first process.

With respect to claim 88, there is a trough between Boutros et al's bypass (810) and the contact (818), and thus, there is a trough between first and second portions as here claimed.

With respect to claims 93, 94, 100, and 109, Boutros et al's contact (818) reads on the instant planar lateral conduction layer deposited over the sequence of layers in the second region. The uppermost GaAs cap of the bypass diode reads on the lateral conduction layer in the first region that is separated from the lateral conduction layer in the first region.

With respect to claim 98, and as clearly seen in said Figure 8, the Ge substrate (802) forms an electrical connection path between the multijunction solar cell and the bypass diode.

Boutros et al teaches the limitations of the instant claims other than the difference which is discussed below

With respect to claims 65 and 86 (and their dependent claims), and also with respect to claims 99 and 108, Boutros et al does not specifically teach that said connecting contact (816) can be made from metal (i.e., instant metal layer). However, as shown by reference sign (1436) in Figure 14B of Ho et al, it is well-known and conventional in the solar cell art to form connecting solar cell contacts from metal (see

also page 8, lines 18-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have prepared Boutros et al's connecting contact (816) from metal because it is well-known and conventional in the art to do so, as shown by Ho et al.

Double Patenting

18. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

19. Claims 37-73 and 86-111 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-35 of U.S. Patent No. 6,864,414. Although the conflicting claims are not identical, they are not patentably distinct from each other because although not of the same scope as the instant claims, the claims of said copending application are anticipatory of the instant claims.

20. Claims 47-59, 61, 65-68, 70, and 90-111 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 48-98 of copending Application No. 10/723,456. Although the conflicting

claims are not identical, they are not patentably distinct from each other because although not of the same scope as the instant claims, the claims of said copending application are anticipatory of the instant claims.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

21. Claims 47-59, 61, 65-68, 70, and 90-111 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-35 of U.S. Patent No. 6,680,432. Although the conflicting claims are not identical, they are not patentably distinct from each other because although not of the same scope as the instant claims, the claims of said patent are anticipatory of the instant claims.

Response to Arguments

22. Applicant's arguments filed May 20, 2005 have been fully considered but they are not persuasive.

Applicant argues that Applicant argues that with respect to claims 47, 90, 93, and 107, Boutros et al "fails to disclose an integral semiconductor body with two regions, with one region forming a solar cell and another region forming a support structure." Applicant argues that Figure 8 of Boutros et al merely shows a single region with solar cells and a bypass diode, and also cites col. 7, lines 51-53 and col. 7, lines 62-65 of Boutros et al. However, Applicant's arguments are not deemed to be persuasive because Boutros et al teaches a multijunction solar cell comprising a Ge substrate (802); a first region including the N and P GaAs layers (804) which form a first junction of the multijunction solar cell and the N and P GaInP layers (806) which form a second

junction of the multijunction solar cell, wherein this first region includes the portion of said N and P GaAs layers (804) and the portion of the N and P GaInP layers (806) not directly below, but to the right of the GaAs cap layer. In a second region, the portions of corresponding N and P GaAs layers (804) and N and P GaInP layers (806) directly below the GaAs Cap support the bypass diode (810) to protect the cell against reverse biasing (see also col. 1, lines 16-22; and col. 7, lines 47-65). Said first and second regions in said Figure 8 clearly are laterally spaced apart, as in claims 47 and 90. With respect to claims 66, 68, 70, 97, 107, when the GaAs P^{++} layer is considered the lateral conduction layer, then the bypass diode above it reads on the instant etch stop layer.

Applicant argues that the bottom layer of Boutros et al's bypass diode has opposite polarity from the top layer of the solar cell. However, this argument is not deemed to be persuasive because in Boutros et al's Figure 8, it is the Examiner's position that the GaAs N^{++} layer can be considered to by the lower layer of the bypass diode, and thus, has the same polarity as the upper N-type GaInP layer of the upper solar cell. Indeed, as seen in Boutros et al's Figures 2A, 3A, and 4A, the bottom layer of the bypass diode (210, 310, 410) is N^{++} and is the same polarity, i.e., N-type, as the top layer (208, 308, 408) of the solar cell.

Applicant argues that they have amended the claims to distinguish over JP '397 by indicating that "the bypass device and the subcell have identical sequence of layers with substantially the same thickness and form an integral semiconductor body." However, this argument is not deemed to be persuasive because it is seen that JP '397's multijunction solar cell solar cell in Figure 1 has transparent electrode (107)

followed by collection electrode (108). This is the same sequence as in the bypass diode, which has transparent electrode (107D) followed by collection electrode (108D). JP '397's multijunction solar cell and bypass diode form an integral semiconductor body on the substrate (103).

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan Diamond whose telephone number is 571-272-1338. The examiner can normally be reached on Monday through Friday, 5:30 a.m. to 2:00 p.m. ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alan Diamond
Primary Examiner
Art Unit 1753

Alan Diamond
August 4, 2005